What is claimed is:

1. A pulse generator comprising a plurality of unit cells, wherein an n^{th} unit cell (n is a natural number more than 2) generates a pulse in response to a divided-by-N clock signal (N is a natural number), a signal output from an $(n-1)^{th}$ unit cell and a signal output from an $(n+1)^{th}$ unit cell.

2. The pulse generator of claim 1, wherein the n^{th} unit cell is reset or generates the pulse, the width of the pulse being equivalent to the width of the divided-by-N clock signal, based on the logic level of the signal output from the $(n-1)^{th}$ unit cell and the logic level of the signal output from the $(n+1)^{th}$ unit cell.

3. The pulse generator of claim 1, wherein phases of the signal output from the $(n-1)^{th}$ unit cell and the signal output from the $(n+1)^{th}$ unit cell are changed with a time difference.

4. The pulse generator of claim 1, wherein the n^{th} unit cell comprises:

a first NAND gate that NANDs the signal output from the $(n-1)^{th}$ unit cell and the signal output from the $(n+1)^{th}$ unit cell;

a first inverter that inverts a signal output from the first NAND gate;

a second NAND gate that NANDs the divided-by-N clock signal and a signal output from the first inverter;

a second inverter that inverts a signal output from the second NAND gate and outputs the pulse as an inverted signal; and

a latch that latches a reset signal and the signal output from the second NAND gate.

5. The pulse generator of claim 4, wherein the second NAND gate comprises:

first and second positive metal oxide semiconductor (PMOS) transistors; and

first and second negative metal oxide semiconductor (NMOS) transistors,

wherein the divided-by-N clock signal is input to a gate of the first PMOS transistor and a gate of the first NMOS transistor, and a signal output from the first inverter is input to a gate of the second PMOS transistor and a gate of the second NMOS transistor.

6. A pulse generator comprising a plurality of unit cells,

wherein a divided-by-N clock signal (N is a natural number), a signal output from a second output terminal of an n-1th unit cell (n is a natural number more than 2), and a signal output from a third output terminal of an n+1th unit cell are input to a first input terminal, a second input terminal, and a third input terminal of an nth unit cell of the plurality of unit cells,

wherein the nth unit cell outputs a pulse whose width is equivalent to the width of the divided-by-N clock signal to a first output terminal of the nth unit cell in response to the signals that are input to the first, second and third input terminals of the nth unit cell.

7. The pulse generator of claim 6, wherein the nth unit cell is reset or outputs the pulse whose width is equivalent to the width of the divided-by-N clock signal to the first output terminal of the nth unit cell, based on the logic level of the signal output from the third output terminal of the (n+1)th unit cell.

8. The pulse generator of claim 6, wherein phases of the signal output from the second output terminal of the n-1th unit cell and the signal output from the third output terminal of the n+1th unit cell are changed with a time difference.

9. The pulse generator of claim 6, wherein the nth unit cell comprises:

a first NAND gate that NANDs the signal which is output from the n-1th unit cell and input to the second input terminal of the nth unit cell, and the signal which is output from the n+1th unit cell and input to the third input terminal of the nth unit cell;

a first inverter that inverts a signal output from the first NAND gate;

a second NAND gate that NANDs the divided-by-N clock signal input to the first input terminal of the n^{th} unit cell and a signal output from the first inverter;

a second inverter that inverts a signal output from the second NAND gate and outputs an inverted signal as the output signal of the n^{th} unit cell; and

a latch that latches a reset signal, and a signal output from the second NAND gate.

10. The pulse generator of claim 9, wherein the second NAND gate comprises:

first and second PMOS transistors; and

first and second NMOS transistors,

wherein the divided-by-N clock signal is input to a gate of the first PMOS transistor and a gate of the first NMOS transistor, and the signal output from the first inverter is input to a gate of the second PMOS transistor and a gate of the second NMOS transistor.

11. The pulse generator of claim 6, wherein the n^{th} unit cell comprises:

a first NAND gate that NANDs the signal which is output from the $n\text{-}1^{th}$ unit cell and input via the second input terminal of the n^{th} unit cell, and the signal which is output from the $n+1^{th}$ unit cell and input via the third input terminal of the n^{th} unit cell;

a first inverter that inverts a signal output from the first NAND gate;

a second NAND gate that NANDs the divided-by-N clock signal input via the first input terminal of the n^{th} unit cell and a signal output from the first inverter;

a second inverter that inverts a signal output from the second NAND gate and outputs an inverted signal as an output signal of the n^{th} unit cell;

a first transmission circuit that responds to the signal output from the second NAND gate and the signal output from the second inverter;

a second transmission circuit that responds to the signal output from the second NAND gate and the signal output from the second inverter;

a third NAND gate that NANDs a reset signal and a signal output from the shared node and outputs the result of NAND to the third output terminal of the n^{th} unit cell; and

a third inverter that inverts the signal output from the third NAND gate and outputs an inverted signal to the second output terminal of the n^{th} unit cell.

12. The pulse generator of claim 11, wherein the second NAND gate comprises:

first and second PMOS transistors; and

first and second NMOS transistors,

wherein the divided-by-N clock signal input to the first input terminal of the n^{th} unit cell is input to a gate of the first PMOS transistor and a gate of the first NMOS transistor, and the signal output from the second inverter is input to a gate of the second PMOS transistor and a gate of the second NMOS transistor.

13. A pulse generator comprising:

a first NAND gate that NANDs a first input signal and a second input signal;

a first inverter that inverts a signal output from the first NAND gate;

a second NAND gate that NANDs a divided-by-N clock signal and a signal output from the first inverter;

a second inverter that inverts a signal output from the second NAND gate; and

a latch that latches a reset signal and the signal output from the second NAND gate.

14 The pulse generator of claim 13, wherein the second inverter generates a pulse corresponding to the divided-by-N clock signal in response to the second input signal.

15. The pulse generator of claim 13, wherein phases of the first and second input signals are changed with a time difference.

16. A pulse generator comprising:

a first NAND gate that NANDs a first input signal and a second input signal input to a second input terminal;

a first inverter that inverts a signal output from the first NAND gate;

a second NAND gate that NANDs a divided-by-N clock signal input to a first input terminal and a signal output from the first inverter;

a second inverter;

a first transmission circuit that responds to a signal output from the second NAND gate and a signal output from the second inverter;

a second transmission circuit that responds to the signal output from the second NAND gate and the signal output from the second inverter;

a third NAND gate that NANDs a reset signal and a signal output from the shared node and outputs the result of NAND to a third output terminal; and

a third inverter.

17. The pulse generator of claim 16, wherein the second inverter generates a pulse whose width is equivalent to the width of the divided-by-N clock signal in response to the second input signal.

18. The pulse generator of claim 16, wherein phases of the first and second input signals are changed with a time difference.